INCREMENTAL REDUNDANCY TRANSMISSION IN A MIMO COMMUNICATION SYSTEM

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to U.S. Provisional Patent Application Serial No. 60/501,777, filed September 9, 2003, and U.S. Provisional Patent Application Serial No. 60/531,391 filed December 19, 2003, which are incorporated herein by reference in their entirety.

BACKGROUND

I. Field

[0002] The present invention relates generally to communication, and more specifically to techniques for transmitting data in a multiple-input multiple-output (MIMO) communication system.

II. Background

[0003] A MIMO system employs multiple (N_T) transmit antennas and multiple (N_R) receive antennas for data transmission and is denoted as an (N_T , N_R) system. A MIMO channel formed by the N_T transmit and N_R receive antennas may be decomposed into N_S spatial channels, where $N_S \leq \min\{N_T, N_R\}$. The MIMO system can provide increased transmission capacity if the N_S spatial channels created by the multiple transmit and receive antennas are used for data transmission.

[0004] A major challenge in a MIMO system is selecting a suitable rate for data transmission based on channel conditions. A "rate" may indicate a particular data rate or information bit rate, a particular coding scheme, a particular modulation scheme, a particular data packet size, and so on. The goal of the rate selection is to maximize throughput on the N_S spatial channels while meeting certain quality objectives, which may be quantified by a particular packet error rate (e.g., 1% PER).

[0005] The transmission capacity of a MIMO channel is dependent on the signal-to-noise-and-interference ratios (SNRs) achieved by the N_S spatial channels. The SNRs are in turn dependent on the channel conditions. In one conventional MIMO system, a transmitter encodes, modulates, and transmits data in accordance with a rate that is

selected based on a model of a static MIMO channel. Good performance can be achieved if the model is accurate and if the MIMO channel is relatively static (i.e., does not change over time). In another conventional MIMO system, a receiver estimates the MIMO channel, selects a suitable rate based on the channel estimates, and sends the selected rate to the transmitter. The transmitter then processes and transmits data in accordance with the selected rate. The performance of this system is dependent on the nature of the MIMO channel and the accuracy of the channel estimates.

[0006] For both conventional MIMO systems described above, the transmitter typically processes and transmits each data packet at the rate selected for that data packet. The receiver decodes each data packet transmitted by the transmitter and determines whether the packet is decoded correctly or in error. The receiver may send back an acknowledgment (ACK) if the packet is decoded correctly or a negative acknowledgment (NAK) if the packet is decoded in error. The transmitter may retransmit each data packet decoded in error by the receiver, in its entirety, upon receiving a NAK from the receiver for the packet.

[0007] The performance of both MIMO systems described above is highly dependent on the accuracy of the rate selection. If the selected rate for a data packet is too conservative (e.g., because the actual SNR is much better than the SNR estimate), then excessive system resources are expended to transmit the data packet and channel capacity is underutilized. Conversely, if the selected rate for the data packet is too aggressive, then the packet may be decoded in error by the receiver and system resources may be expended to retransmit the data packet. Rate selection for a MIMO system is challenging because of (1) greater complexity in the channel estimation for a MIMO channel and (2) the time-varying and independent nature of the multiple spatial channels of the MIMO channel.

[0008] There is therefore a need in the art for techniques to efficiently transmit data in a MIMO system and which do not require accurate rate selection in order to achieve good performance.

SUMMARY

[0009] Techniques are provided herein for performing incremental redundancy (IR) transmission in a MIMO system. Initially, a receiver or a transmitter in the MIMO system estimates a MIMO channel and selects a suitable rate for data transmission on

the MIMO channel. The transmitter is provided with the selected rate if the receiver performs the rate selection.

[0010] The transmitter processes (e.g., encodes, partitions, interleaves, and modulates) a data packet based on the selected rate and obtains multiple (N_B) data symbol blocks for the data packet. The first data symbol block typically contains sufficient information to allow the receiver to recover the data packet under favorable channel conditions. Each of the remaining data symbol blocks contains additional redundancy to allow the receiver to recover the data packet under less favorable channel conditions. The transmitter transmits the first data symbol block from N_T transmit antennas to N_R receive antennas at the receiver. The transmitter thereafter transmits remaining ones of the N_B data symbol blocks, one block at a time, until the data packet is recovered correctly by the receiver or all of the N_B blocks are transmitted.

[0011] If multiple (N_P) data symbol blocks for N_P data packets are to be transmitted simultaneously from the N_T transmit antennas, then the transmitter further processes these N_P data symbol blocks such that the N_P data packets experience similar channel conditions. This allows a single rate to be used for all data packets transmitted simultaneously over the MIMO channel.

[0012] The receiver obtains a received symbol block for each data symbol block transmitted by the transmitter. The receiver "detects" each received symbol block to obtain a detected symbol block, which is an estimate of the corresponding data symbol block. The receiver then processes (e.g., demodulates, deinterleaves, re-assembles, and decodes) all detected symbol blocks obtained for the data packet and provides a decoded packet. The receiver may send back an ACK if the decoded packet is correctly decoded and a NAK if the decoded packet is in error. If the decoded packet is in error, then the receiver repeats the processing when another received symbol block is obtained for another data symbol block transmitted by the transmitter.

[0013] The receiver may also recover the data packet using an iterative detection and decoding (IDD) scheme. For the IDD scheme, whenever a new received symbol block is obtained for the data packet, detection and decoding are iteratively performed multiple (N_{dd}) times on all received symbol blocks to obtain the decoded packet. A detector performs detection on all received symbol blocks and provides detected symbol blocks. A decoder performs decoding on all detected symbol blocks and provides

decoder *a priori* information, which is used by the detector in a subsequent iteration. The decoded packet is generated based on decoder output for the last iteration.

[0014] Various aspects and embodiments of the invention are described in further detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The features and nature of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

[0016] FIG. 1 shows a block diagram of a transmitter and a receiver in a MIMO system that implements IR transmission;

[0017] FIG. 2 shows a process for sending and receiving an IR transmission in the MIMO system;

[0018] FIG. 3 shows a timing diagram that illustrates the IR transmission;

[0019] FIG. 4A shows a transmit (TX) data processor at the transmitter;

[0020] FIG. 4B shows a Turbo encoder within the TX data processor;

[0021] FIG. 5 illustrates the processing of one data packet by the TX data processor;

[0022] FIGS. 6A through 6D show four embodiments of a TX spatial processor at the transmitter;

[0023] FIGS. 7A and 7B show the demultiplexing of one data symbol block and two data symbol blocks, respectively, for an exemplary MIMO-OFDM system;

[0024] FIG. 8A shows one embodiment of the receiver;

[0025] FIG. 8B shows a receive (RX) data processor at the receiver in FIG. 8A;

[0026] FIG. 9A shows a receiver that implements iterative detection and decoding; and

[0027] FIG. 9B shows a Turbo decoder.

DETAILED DESCRIPTION

[0028] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any embodiment or design described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments or designs.

[0029] For a MIMO system with N_S spatial channels, N_P data packets may be transmitted simultaneously from the N_T transmit antennas, where $1 \leq N_P \leq N_S$. A single rate may

be used for all data packets transmitted simultaneously, regardless of the value for N_P. The use of a single rate can simplify the processing at both the transmitter and the receiver in the MIMO system.

[0030] **FIG. 1** shows a block diagram of a transmitter 110 and a receiver 150 in a MIMO system 100 that implements IR transmission. At transmitter 110, a TX data processor 120 receives data packets from a data source 112. TX data processor 120 processes (e.g., formats, encodes, partitions, interleaves, and modulates) each data packet in accordance with a rate selected for that packet to obtain N_B blocks of data symbols for the packet, where $N_B > 1$ and may be dependent on the selected rate. The selected rate for each data packet may indicate the data rate, coding scheme or code rate, modulation scheme, packet size, number of data symbol blocks, and so on, for that packet, which are indicated by the various controls provided by a controller 140. For IR transmission, the N_B data symbol blocks for each data packet are transmitted one block at a time until the packet is decoded correctly by receiver 150 or all N_B data symbol blocks have been transmitted.

[0031] A TX spatial processor 130 receives the data symbol blocks and performs the necessary processing to transmit each data symbol block from all N_T transmit antennas in one time slot (or simply, "slot"). A slot is a predetermined time period for MIMO system 100. TX spatial processor 130 may perform demultiplexing, spatial processing, and so on, as described below. For each slot, TX spatial processor 130 processes one data symbol block, multiplexes in pilot symbols as appropriate, and provides N_T sequences of transmit symbols to a transmitter unit (TMTR) 132. Each transmit symbol may be for a data symbol or a pilot symbol.

[0032] Transmitter unit 132 receives and conditions (e.g., converts to analog, frequency upconverts, filters, and amplifies) the N_T transmit symbol sequences to obtain N_T modulated signals. Each modulated signal is then transmitted from a respective transmit antenna (not shown in FIG. 1) and via the MIMO channel to receiver 150. The MIMO channel distorts the N_T transmitted signals with a channel response of $\underline{\mathbf{H}}$ and further degrades the transmitted signals with additive white Gaussian noise and possibly interference from other transmitters.

[0033] At receiver 150, the N_T transmitted signals are received by each of N_R receive antennas (not shown in FIG. 1), and the N_R received signals from the N_R receive antennas are provided to a receiver unit (RCVR) 154. Receiver unit 154 conditions,

digitizes, and pre-processes each receive signal to obtain a sequence of received symbols for each slot. Receiver unit 154 provides N_R received symbol sequences (for data) to an RX spatial processor 160 and received pilot symbols (for pilot) to a channel estimator 172. RX spatial processor 160 processes (e.g., detects and multiplexes) the N_R received symbol sequences for each slot to obtain a detected symbol block, which is an estimate of the data symbol block sent by transmitter 110 for that slot.

[0034] An RX data processor 170 receives all detected symbol blocks that have been received for the data packet being recovered (i.e., the "current" packet), processes (e.g., demodulates, deinterleaves, re-assembles, and decodes) these detected symbol blocks in accordance with the selected rate, and provides a decoded packet, which is an estimate of the data packet sent by transmitter 110. RX data processor 170 also provides the status of the decoded packet, which indicates whether the packet is decoded correctly or in error.

[0035] Channel estimator 172 processes the received pilot symbols and/or received data symbols to obtain channel estimates (e.g., channel gain estimates and SNR estimates) for the MIMO channel. A rate selector 174 receives the channel estimates and selects a rate for the next data packet to be transmitted to receiver 150. A controller 180 receives the selected rate from rate selector 174 and the packet status from RX data processor 170 and assembles feedback information for transmitter 110. The feedback information may include the selected rate for the next packet, an ACK or a NAK for the current packet, and so on. The feedback information is processed by a TX data/spatial processor 190, further conditioned by a transmitter unit 192, and transmitted via a feedback channel to transmitter 110.

[0036] At transmitter 110, the signal(s) transmitted by receiver 150 are received and conditioned by a receiver unit 146 and further processed by an RX spatial/data processor 148 to recover the feedback information sent by receiver 150. Controller 140 receives the recovered feedback information, uses the selected rate to process the next data packet to be sent to receiver 150, and uses the ACK/NAK to control the IR transmission of the current packet.

[0037] Controllers 140 and 180 direct the operation at transmitter 110 and receiver 150, respectively. Memory units 142 and 182 provide storage for program codes and data used by controllers 140 and 180, respectively. Memory units 142 and 182 may be

internal to controllers 140 and 180, as shown in FIG. 1, or external to these controllers. The processing units shown in FIG. 1 are described in detail below.

[0038] **FIG. 2** shows a flow diagram of a process 200 for sending and receiving an IR transmission in the MIMO system. Initially, the receiver estimates the MIMO channel based on pilot and/or data symbols received from the transmitter (step 210). The receiver selects a single rate for data transmission on the MIMO channel based on the channel estimates and sends the selected rate to the transmitter (step 212). The transmitter receives the selected rate and encodes a data packet in accordance with the selected rate to obtain a coded packet (step 220). The transmitter then partitions the coded packet into N_B subpackets, where N_B may also be determined by the selected rate, and further processes each subpacket to obtain a corresponding data symbol block (also in step 220). The transmitter transmits one data symbol block at a time from the N_T transmit antennas until all N_B data symbol blocks are transmitted or an ACK is received from the receiver for the data packet (step 222).

[0039] The receiver receives each transmitted data symbol block via the N_R receive antennas (step 230). Whenever a new data symbol block is received, the receiver detects and decodes all data symbol blocks that have been received for the data packet (step 232). The receiver also checks the decoded packet to determine whether the packet is decoded correctly (good) or in error (erased) (also step 232). If the decoded packet is erased, then the receiver can send a NAK back to the transmitter, which uses this feedback to initiate transmission of the next data symbol block for the data packet. Alternatively, the transmitter can send one data symbol block at a time until an ACK is received from the receiver, which may or may not send back NAKs. The receiver terminates the processing for the data packet if the packet is decoded correctly or if all N_B data symbol blocks have been received for the packet (step 234).

[0040] FIG. 2 shows a specific embodiment for IR transmission in a MIMO system. IR transmission may also be implemented in other manners, and this is within the scope of the invention. IR transmission may be implemented in both frequency division duplex (FDD) and time division duplex (TDD) systems. For an FDD system, the forward MIMO channel and the feedback channel use different frequency bands and are likely to observe different channel conditions. In this case, the receiver can estimate the forward MIMO channel and send back the selected rate, as shown in FIG. 2. For a TDD system, the forward MIMO channel and the feedback channel share the same frequency band

and are likely to observe similar channel conditions. In this case, the transmitter can estimate the MIMO channel based on a pilot sent by the receiver and use this channel estimate to select the rate for data transmission to the receiver. The channel estimation and rate selection may be performed by the receiver, the transmitter, or both.

[0041] **FIG. 3** illustrates IR transmission in the MIMO system. The receiver estimates the MIMO channel, selects a rate r_1, and sends the selected rate to the transmitter in slot 0. The transmitter receives the selected rate from the receiver, processes a data packet (Packet 1) in accordance with the selected rate, and transmits the first data symbol block (Block 1) for the data packet in slot 1. The receiver receives, detects, and decodes the first data symbol block, determines that Packet 1 is decoded in error, and sends back a NAK in slot 2. The transmitter receives the NAK and transmits the second data symbol block (Block 2) for Packet 1 in slot 3. The receiver receives Block 2, detects and decodes the first two data symbol blocks, determines that Packet 1 is still decoded in error, and sends back a NAK in slot 4. The block transmission and NAK response may repeat any number of times. In the example shown in FIG. 3, the transmitter receives a NAK for data symbol block $N_x - 1$ and transmits data symbol block N_x for Packet 1 in slot m, where N_x is less than or equal to the total number of blocks for Packet 1. The receiver receives, detects, and decodes all N_x data symbol blocks received for Packet 1, determines that the packet is decoded correctly, and sends back an ACK in slot $m+1$. The receiver also estimates the MIMO channel, selects a rate r_2 for the next data packet, and sends the selected rate to the transmitter in slot $m+1$. The transmitter receives the ACK for data symbol block N_x and terminates the transmission of Packet 1. The transmitter also processes the next data packet (Packet 2) in accordance with the selected rate, and transmits the first data symbol block (Block 1) for Packet 2 in slot $m+2$. The processing at the transmitter and receiver continues in the same manner for each data packet transmitted via the MIMO channel.

[0042] For the embodiment shown in FIG. 3, there is a delay of one slot for the ACK/NAK response from the receiver for each block transmission. To improve channel utilization, multiple data packets may be transmitted in an interlaced manner. For example, data packets for one traffic channel may be transmitted in odd-numbered slots and data packets for another traffic channel may be transmitted in even-numbered slots. More than two traffic channels may also be interlaced if the ACK/NAK delay is longer than one slot.

1. Transmitter

[0043] **FIG. 4A** shows a block diagram of an embodiment of TX data processor 120 within transmitter 110. TX data processor 120 receives data packets, processes each packet based on its selected rate, and provides N_B data symbol blocks for the packet. **FIG. 5** illustrates the processing of one data packet by TX data processor 120.

[0044] Within TX data processor 120, a cyclic redundancy check (CRC) generator 412 receives a data packet, generates a CRC value for the data packet, and appends the CRC value to the end of the data packet to form a formatted packet. The CRC value is used by the receiver to check whether the packet is decoded correctly or in error. Other error detection codes may also be used instead of CRC. A forward error correction (FEC) encoder 414 then encodes the formatted packet in accordance with a coding scheme or code rate indicated by the selected rate and provides a coded packet or "codeword". The encoding increases the reliability of the data transmission. FEC encoder 414 may implement a block code, a convolutional code, a Turbo code, some other code, or a combination thereof.

[0045] **FIG. 4B** shows a block diagram of a parallel concatenated convolutional encoder (or Turbo encoder) 414a, which may be used for FEC encoder 414 in FIG. 4A. Turbo encoder 414a includes two constituent convolutional encoders 452a and 452b, a code interleaver 454, and a multiplexer (MUX) 456. Code interleaver 454 interleaves the data bits in the formatted packet (denoted as $\{d\}$) in accordance with a code interleaving scheme. Constituent encoder 452a receives and encodes the data bits with a first constituent code and provides first parity bits (denoted as $\{c_{p1}\}$). Similarly, constituent encoder 452b receives and encodes the interleaved data bits from code interleaver 454 with a second constituent code and provides second parity bits (denoted as $\{c_{p2}\}$). Constituent encoders 452a and 452b may implement two recursive systematic constituent codes with code rates of R_1 and R_2, respectively, where R_1 may or may not be equal to R_2. Multiplexer 456 receives and multiplexes the data bits and the parity bits from constituent encoders 452a and 452b and provides the coded packet of code bits (denoted as $\{c\}$). The coded packet includes the data bits $\{d\}$, which are also referred to as systematic bits and denoted as $\{c_{data}\}$, followed by the first parity bits $\{c_{p1}\}$, and then followed by the second parity bits $\{c_{p2}\}$.

[0046] Referring back to FIG. 4A, a partitioning unit 416 receives and partitions the coded packet into N_B coded subpackets, where N_B may be dependent on the selected rate and indicated by a partitioning control from controller 140. The first coded subpacket typically contains all of the systematic bits and zero or more parity bits. This allows the receiver to recover the data packet with just the first coded subpacket under favorable channel conditions. The other $N_B - 1$ coded subpackets contain the remaining first and second parity bits. Each of these $N_B - 1$ coded subpackets typically contains some first parity bits and some second parity bits, with the parity bits being taken across the entire data packet. For example, if $N_B = 8$ and the remaining first and second parity bits are given indices starting with 0, then the second coded subpacket may contain bits 0, 7, 14, ... of the remaining first and second parity bits, the third coded subpacket may contain bits 1, 8, 15, ... of the remaining first and second parity bits, and so on, and the eighth and last coded subpacket may contain bits 6, 13, 20, ... of the remaining first and second parity bits. Improved decoding performance may be achieved by spreading the parity bits across the other $N_B - 1$ coded subpackets.

[0047] A channel interleaver 420 includes N_B block interleavers 422a through 422nb that receive the N_B coded subpackets from partitioning unit 416. Each block interleaver 422 interleaves (i.e., reorders) the code bits for its subpacket in accordance with an interleaving scheme and provides an interleaved subpacket. The interleaving provides time, frequency, and/or spatial diversity for the code bits. A multiplexer 424 couples to all N_B block interleavers 422a through 422nb and provides the N_B interleaved subpackets, one subpacket at a time and if directed an IR transmission control from controller 140. In particular, multiplexer 424 provides the interleaved subpacket from block interleaver 422a first, then the interleaved subpacket from block interleaver 422b next, and so on, and the interleaved subpacket from block interleaver 422nb last. Multiplexer 424 provides the next interleaved subpacket if a NAK is received for the data packet. All N_B block interleavers 422a through 422nb can be purged whenever an ACK is received.

[0048] A symbol mapping unit 426 receives the interleaved subpackets from channel interleaver 420 and maps the interleaved data in each subpacket to modulation symbols. The symbol mapping is performed in accordance with a modulation scheme indicated by the selected rate. The symbol mapping may be achieved by (1) grouping sets of B bits to form B-bit binary values, where $B \geq 1$, and (2) mapping each B-bit binary value

to a point in a signal constellation having 2^B points. This signal constellation corresponds to the selected modulation scheme, which may be BPSK, QPSK, 2^B-PSK, 2^B-QAM, and so on. As used herein, a "data symbol" is a modulation symbol for data, and a "pilot symbol" is a modulation symbol for pilot. Symbol mapping unit 426 provides a block of data symbols for each coded subpacket, as shown in FIG. 5.

[0049] For each data packet, TX data processor 120 provides N_B data symbol blocks, which collectively include N_{SYM} data symbols and can be denoted as $\{s\} = [s_1 \ s_2 \ \ldots \ s_{N_{SYM}}]$. Each data symbol s_i, where $i = 1 \ldots N_{SYM}$, is obtained by mapping B code bits as follows: $s_i = \text{map}\ (\underline{\mathbf{b}}_i)$ where $\underline{\mathbf{b}}_i = [b_{i,1} \ b_{i,2} \ \ldots \ b_{i,B}]$.

[0050] The IR transmission techniques described herein may be implemented in a single-carrier MIMO system that utilizes one carrier for data transmission and a multi-carrier MIMO system that utilizes multiple carriers for data transmission. Multiple carriers may be provided by orthogonal frequency division multiplexing (OFDM), other multi-carrier modulation techniques, or some other constructs. OFDM effectively partitions the overall system bandwidth into multiple (N_F) orthogonal subbands, which are also commonly referred to as tones, bins, or frequency channels. With OFDM, each subband is associated with a respective carrier that may be modulated with data.

[0051] The processing performed by TX spatial processor 130 and transmitter unit 132 within transmitter 110 is dependent on whether one or multiple data packets are transmitted simultaneously and whether one or multiple carriers are used for data transmission. Some exemplary designs for these two units are described below. For simplicity, the following description assumes a full rank MIMO channel with $N_S = N_T \leq N_R$. In this case, one modulation symbol may be transmitted from each of the N_T transmit antennas for each subband in each symbol period.

[0052] **FIG. 6A** shows a block diagram of a TX spatial processor 130a and a transmitter unit 132a, which may be used for IR transmission of one packet at a time in a single-carrier MIMO system. TX spatial processor 130a includes a multiplexer/ demultiplexer (MUX/DEMUX) 610 that receives a data symbol block and demultiplexes the data symbols in the block into N_T subblocks for the N_T transmit antennas. Multiplexer/demultiplexer 610 also multiplexes in pilot symbols (e.g., in a time division multiplex (TDM) manner) and provides N_T transmit symbol sequences for the N_T transmit antennas. Each transmit symbol sequence is designated for transmission from

one transmit antenna in one slot. Each transmit symbol may be for a data symbol or a pilot symbol.

[0053] Transmitter unit 132a includes N_T TX RF units 652a through 652t for the N_T transmit antennas. Each TX RF unit 652 receives and conditions a respective transmit symbol sequence from TX spatial processor 130a to generate a modulated signal. N_T modulated signals from TX RF units 652a through 652t are transmitted from N_T transmit antennas 672a through 672t, respectively.

[0054] **FIG. 6B** shows a block diagram of a TX spatial processor 130b and transmitter unit 132a, which may be used for IR transmission of multiple packets simultaneously in a single-carrier MIMO system. TX spatial processor 130b includes a matrix multiplication unit 620 that receives N_P data symbol blocks for transmission in one slot, where $1 \le N_P \le N_S$. Unit 620 performs matrix multiplication of the data symbols in the N_P blocks with a transmit basis matrix and a diagonal matrix as follows:

$$\underline{\tilde{\mathbf{s}}} = \underline{\mathbf{M}}\underline{\Lambda}\underline{\mathbf{s}} \quad , \qquad \text{Eq (1)}$$

where $\underline{\mathbf{s}}$ is an $\{N_T \times 1\}$ data vector;

$\underline{\tilde{\mathbf{s}}}$ is an $\{N_T \times 1\}$ preconditioned data vector;

$\underline{\mathbf{M}}$ is an $\{N_T \times N_T\}$ transmit basis matrix, which is a unitary matrix; and

$\underline{\Lambda}$ is an $\{N_T \times N_T\}$ diagonal matrix.

[0055] The vector $\underline{\mathbf{s}}$ includes N_T entries for the N_T transmit antennas, with N_P entries being set to N_P data symbols from the N_P blocks and the remaining $N_T - N_P$ entries being set to zero. The vector $\underline{\tilde{\mathbf{s}}}$ includes N_T entries for N_T preconditioned symbols to be sent from the N_T transmit antennas in one symbol period. The transmit basis matrix $\underline{\mathbf{M}}$ allows each data symbol block to be sent from all N_T transmit antennas. This enables all N_P data symbol blocks to experience similar channel conditions and further allows a single rate to be used for all N_P data packets. The matrix $\underline{\mathbf{M}}$ also allows the full power P_{ant} of each transmit antenna to be utilized for data transmission. The matrix $\underline{\mathbf{M}}$ may be defined as $\underline{\mathbf{M}} = \frac{1}{\sqrt{N_T}}\underline{\mathbf{U}}$, where $\underline{\mathbf{U}}$ is a Walsh-Hadamard matrix. The matrix $\underline{\mathbf{M}}$ may also be defined as $\underline{\mathbf{M}} = \frac{1}{\sqrt{N_T}}\underline{\mathbf{V}}$, where $\underline{\mathbf{V}}$ is a discrete Fourier transform (DFT)

matrix with the (k,i)-th entry defined as $v_{m,n} = e^{-j2\pi\frac{(m-1)(n-1)}{N_T}}$, where m is a row index and n is a column index for the matrix $\underline{\mathbf{V}}$, with $m = 1 \ldots N_T$ and $n = 1 \ldots N_T$. The diagonal matrix $\underline{\Lambda}$ may be used to allocate different transmit powers to the N_P data symbol blocks while conforming to the total transmit power constraint of P_{tot} for each transmit antenna. The "effective" channel response observed by the receiver is then $\underline{\mathbf{H}}_{eff} = \underline{\mathbf{H}}\underline{\mathbf{M}}$. This transmission scheme is described in further detail in commonly assigned U.S. Patent Application Serial No. 10/367,234, entitled "Rate Adaptive Transmission Scheme for MIMO Systems," filed February 14, 2003.

[0056] A multiplexer 622 receives the preconditioned symbols from matrix multiplication unit 620, multiplexes in pilot symbols, and provides N_T transmit symbol sequences for the N_T transmit antennas. Transmitter unit 132a receives and conditions the N_T transmit symbol sequences and generates N_T modulated signals.

[0057] **FIG. 6C** shows a block diagram of TX spatial processor 130a and a transmitter unit 132b, which may be used for IR transmission of one packet at a time in a MIMO-OFDM system. Within TX spatial processor 130a, multiplexer/demultiplexer 610 receives and demultiplexes the data symbols, multiplexes in pilot symbols, and provides N_T transmit symbol sequences for the N_T transmit antennas.

[0058] Transmitter unit 132b includes N_T OFDM modulators 660a through 660t and N_T TX RF units 666a through 666t for the N_T transmit antennas. Each OFDM modulator 660 includes an inverse fast Fourier transform (IFFT) unit 662 and a cyclic prefix generator 664. Each OFDM modulator 660 receives a respective transmit symbol sequence from TX spatial processor 130a and groups each set of N_F transmit symbols and zero signal values for the N_F subbands. (Subbands not used for data transmission are filled with zeros.) IFFT unit 662 transforms each set of N_F transmit symbols and zeros to the time domain using an N_F-point inverse fast Fourier transform and provides a corresponding transformed symbol that contains N_F chips. Cyclic prefix generator 664 repeats a portion of each transformed symbol to obtain a corresponding OFDM symbol that contains $N_F + N_{cp}$ chips. The repeated portion is referred to as a cyclic prefix, and N_{cp} indicates the number of chips being repeated. The cyclic prefix ensures that the OFDM symbol retains its orthogonal properties in the presence of multipath delay spread caused by frequency selective fading (i.e., a frequency response that is not flat). Cyclic

prefix generator 664 provides a sequence of OFDM symbols for the sequence of transmit symbols, which is further conditioned by an associated TX RF unit 666 to generate a modulated signal.

[0059] **FIG. 7A** shows the demultiplexing of a data symbol block for an exemplary MIMO-OFDM system with four transmit antennas ($N_T = 4$) and 16 subbands ($N_F = 16$). The data symbol block may be denoted as $\{s\} = [s_1 \; s_2 \; \ldots \; s_{N_{SYM}}]$. For the embodiment shown in FIG. 7A, the demultiplexing is performed such that the first four data symbols s_1 through s_4 in the block are sent on subband 1 of transmit antennas 1 through 4, respectively, the next four data symbols s_5 through s_8 are sent on subband 2 of transmit antennas 1 through 4, respectively, and so on.

[0060] **FIG. 6D** shows a block diagram of a TX spatial processor 130c and transmitter unit 132b, which may be used for IR transmission of multiple packets simultaneously in a MIMO-OFDM system. Within TX spatial processor 130c, a multiplexer/demultiplexer 630 receives N_P data symbol blocks, where $1 \le N_P \le N_S$, and provides the data symbols in each block to different subbands and different transmit antennas, as illustrated below. Multiplexer/demultiplexer 630 also multiplexes in pilot symbols and provides N_T transmit symbol sequences for the N_T transmit antennas.

[0061] **FIG. 7B** shows an embodiment of the multiplexing/demultiplexing of two data symbol blocks ($N_P = 2$) for the exemplary MIMO-OFDM system with four transmit antennas ($N_T = 4$) and 16 subbands. For the first data symbol block, the first four data symbols $s_{1,1}$, $s_{1,2}$, $s_{1,3}$ and $s_{1,4}$ are transmitted on subbands 1, 2, 3 and 4, respectively, of transmit antennas 1, 2, 3 and 4, respectively. The next four data symbols $s_{1,5}$, $s_{1,6}$, $s_{1,7}$ and $s_{1,8}$ wrap around and are transmitted on subbands 5, 6, 7 and 8, respectively, of transmit antennas 1, 2, 3 and 4, respectively. For the second data symbol block, the first four data symbols $s_{2,1}$, $s_{2,2}$, $s_{2,3}$ and $s_{2,4}$ are transmitted on subbands 1, 2, 3 and 4, respectively, of transmit antennas 3, 4, 1 and 2, respectively. The next four data symbols $s_{2,5}$, $s_{2,6}$, $s_{2,7}$ and $s_{2,8}$ wrap around and are transmitted on subbands 5, 6, 7 and 8, respectively, of transmit antennas 3, 4, 1 and 2, respectively. For the embodiment shown in FIG. 7B, the set of N_F frequency-domain values for each transmit antenna for each symbol period includes transmit symbols for some subbands and zeros for other subbands.

[0062] FIG. 7B shows the transmission of two data symbol blocks simultaneously across the N_F subbands and N_T transmit antennas. In general, any number of data symbol blocks may be transmitted simultaneously across the subbands and transmit antennas. For example, one, two, three, or four data symbol blocks may be transmitted simultaneously in FIG. 7B. However, the number of data symbol blocks that may be reliably transmitted at the same time is dependent on the rank of the MIMO channel, so that N_P should be less than or equal to N_S. The transmission scheme shown in FIG. 7B allows for easy adaptation of the transmission of different numbers of data symbol blocks simultaneously based on the rank of the MIMO channel.

[0063] For the embodiment shown in FIG. 7B, each data symbol block is transmitted diagonally across the N_F subbands and from all N_T transmit antennas. This provides both frequency and spatial diversity for all N_P data symbol blocks being transmitted simultaneously, which allows a single rate to be used for all data packets. However, different rates may also be used for different data packets transmitted simultaneously. The use of different rates may provide better performance for some receivers such as, for example, a linear receiver that does not implement the IDD scheme. IR transmission of multiple data packets with different rates simultaneously is described in commonly assigned U.S. Patent Application Serial No. 10/785,292, entitled "Incremental Redundancy Transmission for Multiple Parallel Channels in a MIMO Communication System," filed February 23, 2004.

[0064] The multiplexing/demultiplexing may also be performed in other manners while achieving both frequency and spatial diversity. For example, the multiplexing/demultiplexing may be such that all N_F subbands of each transmit antenna are used to carry transmit symbols. Since the full power of each transmit antenna is limited to P_{ant}, the amount of transmit power available for each transmit symbol is dependent on the number of subbands carrying transmit symbols.

[0065] Referring back to FIG. 6D, transmitter unit 132b receives and conditions the N_T transmit symbol sequences from TX spatial processor 130c and generates N_T modulated signals.

2. Receiver

[0066] **FIG. 8A** shows a block diagram of a receiver 150a, which is one embodiment of receiver 150 in FIG. 1. At receiver 150a, N_R receive antennas 810a through 810r

receive the N_T modulated signals transmitted by transmitter 110 and provide N_R received signals to N_R RX RF units 812a through 812r, respectively, within receiver unit 154. Each RX RF unit 812 conditions and digitizes its received signal and provides a stream of symbols/chips. For a single-carrier MIMO system, OFDM demodulators 814a through 814r are not needed, and each RX RF unit 812 provides a stream of symbols directly to a respective demultiplexer 816. For a MIMO-OFDM system, each RX RF unit 812 provides a stream of chips to a respective OFDM demodulator 814. Each OFDM demodulator 814 performs OFDM demodulation on its stream of chips by (1) removing the cyclic prefix in each received OFDM symbol to obtain a received transformed symbol and (2) transforming each received transformed symbol to the frequency domain with a fast Fourier transform (FFT) to obtain N_F received symbols for the N_F subbands. For both systems, demultiplexers 816a through 816r receive N_R symbol streams from RX RF units 812 or OFDM demodulators 814, provide N_R sequences of received symbols (for data) for each slot to RX spatial processor 160a, and provide received pilot symbols to channel estimator 172.

[0067] RX spatial processor 160a includes a detector 820 and a multiplexer 822. Detector 820 performs spatial or space-time processing (or "detection") on the N_R received symbol sequences to obtain N_T detected symbol sequences. Each detected symbol is an estimate of a data symbol transmitted by the transmitter. Detector 820 may implement a maximal ratio combining (MRC) detector, a linear zero-forcing (ZF) detector (which is also referred to as a channel correlation matrix inversion (CCMI) detector), a minimum mean square error (MMSE) detector, an MMSE linear equalizer (MMSE-LE), a decision feedback equalizer (DFE), or some other detector/equalizer. The detection may be performed based on an estimate of the channel response matrix $\underline{\mathbf{H}}$ if spatial processing is not performed at the transmitter. Alternatively, the detection may be performed based on the effective channel response matrix $\underline{\mathbf{H}}_{eff} = \underline{\mathbf{H}}\underline{\mathbf{M}}$, if the data symbols are pre-multiplied with the transmit basis matrix $\underline{\mathbf{M}}$ at the transmitter for a single-carrier MIMO system. For simplicity, the following description assumes that the transmit basis matrix $\underline{\mathbf{M}}$ was not used.

[0068] The model for a MIMO-OFDM system may be expressed as:

$$\underline{\mathbf{r}}(k) = \underline{\mathbf{H}}(k)\underline{\mathbf{s}}(k) + \underline{\mathbf{n}}(k) \quad , \text{ for } k = 1 \ldots N_F , \qquad \text{Eq (2)}$$

where $\underline{\mathbf{s}}(k)$ is an $\{N_T \times 1\}$ data vector with N_T entries for N_T data symbols transmitted from the N_T transmit antennas on subband k;

$\underline{\mathbf{r}}(k)$ is an $\{N_R \times 1\}$ receive vector with N_R entries for N_R received symbols obtained via the N_R receive antennas on subband k;

$\underline{\mathbf{H}}(k)$ is the $\{N_R \times N_T\}$ channel response matrix for subband k; and

$\underline{\mathbf{n}}(k)$ is a vector of additive white Gaussian noise (AWGN).

The vector $\underline{\mathbf{n}}(k)$ is assumed to have zero mean and a covariance matrix of $\underline{\Lambda}_n = \sigma^2 \underline{\mathbf{I}}$, where σ^2 is the variance of the noise and $\underline{\mathbf{I}}$ is the identity matrix with ones along the diagonal and zeros everywhere else.

[0069] For a MIMO-OFDM system, the receiver performs detection separately for each of the subbands used for data transmission. The following description is for one subband, and for simplicity the subband index k is omitted in the mathematical derivation. The following description is also applicable for a single-carrier MIMO system. For simplicity, the vector $\underline{\mathbf{s}}$ is assumed to include N_T data symbols sent from the N_T transmit antennas.

[0070] The spatial processing by an MRC detector may be expressed as:

$$\hat{\underline{\mathbf{s}}}_{mrc} = \underline{\mathbf{W}}_{mrc}^H \underline{\mathbf{r}} \quad , \qquad \text{Eq (3)}$$

where $\underline{\mathbf{W}}_{mrc}$ is the response of the MRC detector, which is $\underline{\mathbf{W}}_{mrc} = \underline{\mathbf{H}}$;

$\hat{\underline{\mathbf{s}}}_{mrc}$ is an $\{N_T \times 1\}$ vector of detected symbols for the MRC detector; and

"^{H}" denotes the conjugate transpose.

The detected symbol for transmit antenna i may be expressed as $\hat{s}_{mrc,i} = \underline{\mathbf{w}}_{mrc,i}^H \underline{\mathbf{r}}$, where $\underline{\mathbf{w}}_{mrc,i}$ is the i-th column of $\underline{\mathbf{W}}_{mrc}$ and is given as $\underline{\mathbf{w}}_{mrc,i} = \underline{\mathbf{h}}_i$, where $\underline{\mathbf{h}}_i$ is the channel response vector between transmit antenna i and the N_R receive antennas.

[0071] The spatial processing by an MMSE detector may be expressed as:

$$\hat{\underline{\mathbf{s}}}_{mmse} = \underline{\mathbf{W}}_{mmse}^H \underline{\mathbf{r}} \quad , \qquad \text{Eq (4)}$$

where $\underline{\mathbf{W}}_{mmse} = (\underline{\mathbf{H}}\underline{\mathbf{H}}^H + \sigma^2 \underline{\mathbf{I}})^{-1} \underline{\mathbf{H}}$ for the MMSE detector. The MMSE detector response for transmit antenna i may be expressed as $\underline{\mathbf{w}}_{mmse,i} = (\underline{\mathbf{H}}\underline{\mathbf{H}}^H + \sigma^2 \underline{\mathbf{I}})^{-1} \underline{\mathbf{h}}_i$.

[0072] The spatial processing by a zero-forcing detector may be expressed as:

$$\hat{\underline{\mathbf{s}}}_{zf} = \underline{\mathbf{W}}_{zf}^{H}\underline{\mathbf{r}} \ , \qquad \text{Eq (5)}$$

where $\underline{\mathbf{W}}_{zf} = \underline{\mathbf{H}}(\underline{\mathbf{H}}^{H}\underline{\mathbf{H}})^{-1}$ for the zero-forcing detector. The zero-forcing detector response for transmit antenna i may be expressed as $\underline{\mathbf{w}}_{zf} = \underline{\mathbf{h}}_i(\underline{\mathbf{H}}^{H}\underline{\mathbf{H}})^{-1}$.

[0073] For each slot, detector 820 provides N_T detected symbol sequences that correspond to the N_T entries of $\hat{\underline{\mathbf{s}}}$. Multiplexer 822 receives the N_T detected symbol sequences from detector 820 and performs processing complementary to that performed by TX spatial processor 130 at the transmitter. If only one data symbol block is transmitted in each slot, such as for TX spatial processor 130a in FIGS. 6A and 6C, then multiplexer 822 multiplexes the detected symbols in the N_T sequences into one detected symbol block. If multiple data symbol blocks are transmitted in each slot, such as for TX spatial processors 130b and 130c in FIGS. 6B and 6D, respectively, then multiplexer 822 multiplexes and demultiplexes the detected symbols in the N_T sequences into N_P detected symbol blocks (not shown in FIG. 8A). In any case, each detected symbol block is an estimate of a data symbol block transmitted by the transmitter.

[0074] Channel estimator 172 estimates the channel response matrix $\underline{\mathbf{H}}$ for the MIMO channel and the noise floor at the receiver (e.g., based on received pilot symbols) and provides channel estimates to controller 180. Within controller 180, a matrix computation unit 176 derives the detector response $\underline{\mathbf{W}}$ (which may be $\underline{\mathbf{W}}_{mrc}$, $\underline{\mathbf{W}}_{mmse}$, or $\underline{\mathbf{W}}_{zf}$) based on the estimated channel response matrix, as described above, and provides the detector response to detector 820. Detector 820 pre-multiplies the vector $\underline{\mathbf{r}}$ of received symbols with the detector response $\underline{\mathbf{W}}$ to obtain the vector $\hat{\underline{\mathbf{s}}}$ of detected symbols. Rate selector 174 (which is implemented by controller 180 for the receiver embodiment shown in FIG. 8A) performs rate selection based on the channel estimates, as described below. A look-up table (LUT) 184 stores a set of rates supported by the MIMO system and a set of parameter values associated with each rate (e.g., the data rate, packet size, coding scheme or code rate, modulation scheme, and so on for each rate). Rate selector 174 accesses LUT 184 for information used for rate selection.

[0075] **FIG. 8B** shows a block diagram of an RX data processor 170a, which is one embodiment of RX data processor 170 in FIGS. 1 and 8A. Within RX data processor

170a, a symbol demapping unit 830 receives detected symbols blocks from RX spatial processor 160a, one block at a time. For each detected symbol block, symbol demapping unit 830 demodulates the detected symbols in accordance with the modulation scheme used for that block (as indicated by a demodulation control from controller 180) and provides a demodulated data block to a channel deinterleaver 840. Channel deinterleaver 840 includes a demultiplexer 842 and N_B block deinterleavers 844a through 844nb. Prior to receiving a new data packet, block deinterleavers 844a through 844nb are initialized with erasures. An erasure is a value that substitutes for a missing code bit (i.e., one not yet received) and is given appropriate weight in the decoding process. Multiplexer 842 receives demodulated data blocks from symbol demapping unit 830 and provides each demodulated data block to the proper block deinterleaver 844. Each block deinterleaver 844 deinterleaves the demodulated data in its block in a manner complementary to the interleaving performed at the transmitter for that block. If the interleaving is dependent on the selected rate, then controller 180 provides a deinterleaving control to block deinterleavers 844, as indicated by the dashed line.

[0076] Whenever a new data symbol block is received from the transmitter for a data packet, the decoding is performed anew on all blocks received for that packet. A re-assembly unit 848 forms a packet of deinterleaved data for subsequent decoding. The deinterleaved data packet contains (1) deinterleaved data blocks for all data symbol blocks received for the current packet and (2) erasures for data symbol blocks not received for the current packet. Re-assembly unit 848 performs re-assembly in a complementary manner to the partitioning performed by the transmitter, as indicated by a re-assembly control from controller 180.

[0077] An FEC decoder 850 decodes the deinterleaved data packet in a manner complementary to the FEC encoding performed at the transmitter, as indicated by a decoding control from controller 180. For example, a Turbo decoder or a Viterbi decoder may be used for FEC decoder 850 if Turbo or convolutional coding, respectively, is performed at the transmitter. FEC decoder 850 provides a decoded packet for the current packet. A CRC checker 852 checks the decoded packet to determine whether the packet is decoded correctly or in error and provides the status of the decoded packet.

[0078] **FIG. 9A** shows a block diagram of a receiver 150b, which is another embodiment of receiver 150 in FIG. 1. Receiver 150b implements an iterative detection and decoding (IDD) scheme. For clarity, the IDD scheme is described below for the coding scheme shown in FIGS. 4B and 5, which codes a data packet into three parts – systematic bits $\{c_{data}\}$, first parity bits $\{c_{p1}\}$, and second parity bits $\{c_{p2}\}$.

[0079] Receiver 150b includes a detector 920 and an FEC decoder 950 that perform iterative detection and decoding on the received symbols for a data packet to obtain a decoded packet. The IDD scheme exploits the error correction capabilities of the channel code to provide improved performance. This is achieved by iteratively passing *a priori* information between detector 920 and FEC decoder 950 for N_{dd} iterations, where $N_{dd} > 1$, as described below. The *a priori* information indicates the likelihood of the transmitted bits.

[0080] Receiver 150b includes an RX spatial processor 160b and an RX data processor 170b. Within RX spatial processor 160b, a buffer 918 receives and stores the N_R received symbol sequences provided by receiver unit 154 for each slot. Whenever a new data symbol block is received from the transmitter for a data packet, the iterative detection and decoding is performed anew (i.e., from the start) on the received symbols for all blocks received for that packet. Detector 920 performs spatial processing or detection on the N_R received symbol sequences for each received block and provides N_T detected symbol sequences for that block. Detector 920 may implement an MRC detector, a zero-forcing detector, an MMSE detector, or some other detector/equalizer. For clarity, detection with an MMSE detector is described below.

[0081] For an MMSE detector with iterative detection and decoding, the detected symbol $\hat{s}_i$ for transmit antenna i may be expressed:

$$\hat{s}_i = \underline{\mathbf{w}}_i^H \underline{\mathbf{r}} - u_i \quad , \quad \text{for } i = 1 \ldots N_T , \qquad \text{Eq (6)}$$

where $\underline{\mathbf{w}}_i$ and u_i are derived based on an MMSE criterion, which can be expressed as:

$$(\underline{\mathbf{w}}_i, u_i) = \min_{(\underline{\mathbf{w}}_i, u_i)} E[|s_i - \hat{s}_i|^2] \quad . \qquad \text{Eq (7)}$$

The solutions to the optimization problem posed in equation (7) can be expressed as:

$$\underline{\mathbf{w}}_i = (\underline{\mathbf{P}} + \underline{\mathbf{Q}} + \sigma^2 \underline{\mathbf{I}})^{-1} \underline{\mathbf{h}}_i \quad , \text{ and} \qquad \text{Eq (8)}$$

$$u_i = \underline{\mathbf{w}}_i^H \underline{\mathbf{z}} \quad , \qquad \text{Eq (9)}$$

$$\text{with} \quad \underline{\mathbf{P}} = \underline{\mathbf{h}}_i \underline{\mathbf{h}}_i^H \quad , \qquad \text{Eq (10)}$$

$$\underline{\mathbf{Q}} = \underline{\mathbf{H}}_i [E[(\underline{\mathbf{s}}_i - E[\underline{\mathbf{s}}_i])(\underline{\mathbf{s}}_i - E[\underline{\mathbf{s}}_i])^H]] \underline{\mathbf{H}}_i^H = \underline{\mathbf{H}}_i [VAR[\underline{\mathbf{s}}_i]] \underline{\mathbf{H}}_i^H \quad , \text{ and} \qquad \text{Eq (11)}$$

$$\underline{\mathbf{z}} = \underline{\mathbf{H}}_i E[\underline{\mathbf{s}}_i] \quad , \qquad \text{Eq (12)}$$

where $\underline{\mathbf{h}}_i$ is the i-th column of the channel response matrix $\underline{\mathbf{H}}$;

$\underline{\mathbf{H}}_i$ is equal to $\underline{\mathbf{H}}$ with the i-th column set to zero;

$\underline{\mathbf{s}}_i$ is an $\{(N_T - 1) \times 1\}$ vector obtained by removing the i-th element of $\underline{\mathbf{s}}$;

$E[\underline{\mathbf{a}}]$ is the expected values of the entries of vector $\underline{\mathbf{a}}$; and

$VAR[\underline{\mathbf{a}}\underline{\mathbf{a}}^H]$ is a covariance matrix of vector $\underline{\mathbf{a}}$.

The matrix $\underline{\mathbf{P}}$ is the outer product of the channel response vector $\underline{\mathbf{h}}_i$ for transmit antenna i. The matrix $\underline{\mathbf{Q}}$ is the covariance matrix of the interference to transmit antenna i. The vector $\underline{\mathbf{z}}$ is the expected value of the interference to transmit antenna i.

[0082] Equation (6) can be simplified as:

$$\hat{s}_i = \alpha_i s_i + \eta_i \quad , \text{ for } i = 1 \ldots N_T \, , \qquad \text{Eq (13)}$$

where $\alpha_i = \underline{\mathbf{w}}_i^H \underline{\mathbf{h}}_i$ and η_i is a Gaussian noise sample with zero mean and variance of $\nu_i = \underline{\mathbf{w}}_i^H \underline{\mathbf{h}}_i - (\underline{\mathbf{w}}_i^H \underline{\mathbf{h}}_i)^2$. The Gaussian noise sample η_i assumes that the interference from other transmit antennas is Gaussian after the MMSE detector.

[0083] In the following description, the superscript n denotes the n-th detection/decoding iteration and the subscript m denotes the m-th data symbol block received for the current packet being recovered. For the first iteration (i.e., $n = 1$) the detection is based solely on the received symbols since no *a priori* information is available from the FEC decoder. Hence, bits with equal probability of being '1' or '0' are assumed. In this case, equation (8) reduces to a linear MMSE detector, which can be given as

$\underline{\mathbf{w}}_i = (\underline{\mathbf{H}}\underline{\mathbf{H}}^H + \sigma^2\underline{\mathbf{I}})^{-1}\underline{\mathbf{h}}_i$. For each subsequent iteration (i.e., $n > 1$), the *a priori* information provided by the FEC decoder is used by the detector. As the number of iterations increases, the interference reduces and the detector converges to the MRC detector that achieves full diversity.

[0084] For each data symbol block received for the current packet, detector 920 in FIG. 9A performs detection on N_R received symbol sequences for that block and provides N_T detected symbol sequences. A multiplexer 922 multiplexes the detected symbols in the N_T sequences to obtain a detected symbol block, which is provided to RX data processor 170b. The detected symbol block obtained in the n-th detection/decoding iteration for the m-th data symbol block is denoted as $\{\hat{s}_m^n\}$.

[0085] Within RX data processor 170b, a log-likelihood ratio (LLR) computation unit 930 receives the detected symbols from RX spatial processor 160b and computes the LLRs of the B code bits for each detected symbol. Each detected symbol $\hat{s}_i$ is an estimate of the data symbol s_i, which is obtained by mapping B code bits $\underline{\mathbf{b}}_i = [b_{i,1}\ b_{i,2}\ \ldots\ b_{i,B}]$ to a point in a signal constellation. The LLR for the j-th bit of detected symbol $\hat{s}_i$ may be expressed as:

$$x_{i,j} = \log\left[\frac{\Pr(\hat{s}_i \mid b_{i,j} = 1)}{\Pr(\hat{s}_i \mid b_{i,j} = -1)}\right], \qquad \text{Eq (14)}$$

where $b_{i,j}$ is the j-th bit for detected symbol $\hat{s}_i$;

$\Pr(\hat{s}_i \mid b_{i,j} = 1)$ is the probability of detected symbol $\hat{s}_i$ with bit $b_{i,j}$ being 1;

$\Pr(\hat{s}_i \mid b_{i,j} = -1)$ is the probability of detected symbol $\hat{s}_i$ with bit $b_{i,j}$ being -1 (i.e., '0'); and

$x_{i,j}$ is the LLR of bit $b_{i,j}$.

The LLRs $\{x_{i,j}\}$ represent the *a priori* information provided by the detector to the FEC decoder, and are also referred to as the detector LLRs.

[0086] For simplicity, the interleaving is assumed to be such that the B bits for each detected symbol $\hat{s}_i$ are independent. Equation (14) may then be expressed as:

$$x_{i,j} = \log\left[\frac{\sum_{s\in\Omega_{j,1}} \exp\left[\frac{-1}{2\nu_i^2}|\hat{s}_i - \alpha_i s|^2\right]\exp\left[\frac{1}{2}\underline{\mathbf{b}}_i^T(j)\underline{\mathbf{L}}_i(j)\right]}{\sum_{s\in\Omega_{j,-1}} \exp\left[\frac{-1}{2\nu_i^2}|\hat{s}_i - \alpha_i s|^2\right]\exp\left[\frac{1}{2}\underline{\mathbf{b}}_i^T(j)\underline{\mathbf{L}}_i(j)\right]}\right], \qquad \text{Eq (15)}$$

where $\Omega_{j,q}$ is the set of points in the signal constellation whose j-th bit is equal to q,

s is the modulation symbol or point in the set $\Omega_{j,q}$ being evaluated (i.e., the "hypothesized" symbol);

α_i is the gain for transmit antenna i and defined above;

ν_i is the variance of the Gaussian noise sample η_i for detected symbol $\hat{s}_i$;

$\underline{\mathbf{b}}_i$ is the set of B bits for the hypothesized symbol s;

$\underline{\mathbf{b}}_i(j)$ is equal to $\underline{\mathbf{b}}_i$ with the j-th bit removed;

$\underline{\mathbf{L}}_i$ is a set of LLRs obtained from the FEC decoder for the B bits of the hypothesized symbol s;

$\underline{\mathbf{L}}_i(j)$ is equal to $\underline{\mathbf{L}}_i$ with the decoder LLR for the j-th bit removed (i.e., $\underline{\mathbf{L}}_i(j) = [\lambda_{i,1}, \ldots, \lambda_{i,j-1}, \lambda_{i,j+1}, \ldots, \lambda_{i,B}]$); and

"^{T}" denotes the transpose.

[0087] The decoder LLR for the (i, j)-th bit can be expressed as:

$$\lambda_{i,j} = \log\left[\frac{\Pr(b_{i,j} = 1)}{\Pr(b_{i,j} = -1)}\right], \qquad \text{Eq (16)}$$

where $\Pr(b_{i,j} = 1)$ is the probability of bit $b_{i,j}$ being 1; and

$\Pr(b_{i,j} = -1)$ is the probability of bit $b_{i,j}$ being -1.

For the first iteration ($n = 1$), all of the entries of $\underline{\mathbf{L}}_i(j)$ are set to zeros to denote equal probability of each bit being 1 or -1, since no *a priori* information is available for the bit. For each subsequent iteration, the entries of $\underline{\mathbf{L}}_i(j)$ are computed based on the "soft" values for the bits from the FEC decoder. LLR computation unit 930 provides LLRs for the code bits of each detected symbol received from RX spatial processor 160b. The block of LLRs obtained in the n-th detection/decoding iteration for the m-th data symbol block is denoted as $\{x_m^n\}$.

[0088] A channel deinterleaver 940 receives and deinterleaves each block of LLRs from LLR computation unit 930 and provides deinterleaved LLRs for the block. A re-assembly unit 948 forms a packet of LLRs that contains (1) blocks of deinterleaved LLRs from channel deinterleaver 940 for all data symbol blocks received from the transmitter and (2) blocks of zero-value LLRs for data symbol blocks not received. The packet of LLRs for the n-th detection/decoding iteration is denoted as $\{x^n\}$. FEC decoder 950 receives and decodes the packet of LLRs from re-assembly unit 948, as described below.

[0089] **FIG. 9B** shows a block diagram of a Turbo decoder 950a, which may be used for FEC decoders 950 and 850 in FIGS. 9A and 8B, respectively. Turbo decoder 950a performs iterative decoding for a parallel concatenated convolutional code, such as the one shown in FIG. 4B.

[0090] Within Turbo decoder 950a, a demultiplexer 952 receives and demultiplexes the packet of LLRs $\{x^n\}$ from re-assembly unit 948 (which is also denoted as the input LLRs) into data bit LLRs $\{x^n_{data}\}$, first parity bit LLRs $\{x^n_{p1}\}$, and second parity bit LLRs $\{x^n_{p2}\}$. A soft-input soft-output (SISO) decoder 954a receives the data bit LLRs $\{x^n_{data}\}$ and the first parity bit LLRs $\{x^n_{p1}\}$ from demultiplexer 952 and deinterleaved data bit LLRs $\{\tilde{x}_{data2}\}$ from a code deinterleaver 958. SISO decoder 954a then derives new LLRs for the data and first parity bits, $\{x_{data1}\}$ and $\{x^{n+1}_{p1}\}$, based on the first constituent convolutional code. A code interleaver 956 interleaves the data bit LLRs $\{x_{data1}\}$ in accordance with the code interleaving scheme used at the transmitter and provides interleaved data bit LLRs $\{\tilde{x}_{data1}\}$. Similarly, a SISO decoder 954b receives the data bit LLRs $\{x^n_{data}\}$ and the second parity bit LLRs $\{x^n_{p2}\}$ from demultiplexer 952 and the interleaved data bit LLRs $\{\tilde{x}_{data1}\}$ from code interleaver 956. SISO decoder 954b then derives new LLRs for the data and second parity bits, $\{x_{data2}\}$ and $\{x^{n+1}_{p2}\}$, based on the second constituent convolutional code. Code deinterleaver 958 deinterleaves the data bit LLRs $\{x_{data2}\}$ in a complementary manner to the code interleaving and provides the deinterleaved data bit LLRs $\{\tilde{x}_{data2}\}$. SISO decoders 954a and 954b may implement a BCJR SISO maximum *a posteriori* (MAP) algorithm or its

lower complexity derivatives, a soft-output Viterbi (SOV) algorithm, or some other decoding algorithm, which are known in the art.

[0091] The decoding by SISO decoders 954a and 954b is iterated N_{dec} times for the current detection/decoding iteration n, where $N_{dec} \geq 1$. After all N_{dec} decoding iterations have been completed, a combiner/multiplexer 960 receives the final data bit LLRs $\{x_{data1}\}$ and the final first parity bit LLRs $\{x_{p1}^{n+1}\}$ from SISO decoder 954a, the deinterleaved final data bit LLRs $\{\tilde{x}_{data2}\}$ from code deinterleaver 958, and the final second parity bit LLRs $\{x_{p2}^{n+1}\}$ from SISO decoder 954b. Combiner/multiplexer 960 then computes decoder LLRs $\{x_{dec}^{n+1}\}$ for the next detection/decoding iteration $n+1$ as follows: $\{x_{dec}^{n+1}\} = \{x_{data1} + \tilde{x}_{data2}, x_{p1}^{n+1}, x_{p2}^{n+1}\}$. The decoder LLRs $\{x_{dec}^{n+1}\}$ correspond to $\lambda_{i,j}$ in equation (16) and represent the *a priori* information provided by the FEC decoder to the detector.

[0092] After all N_{dd} detection/decoding iterations have been completed, combiner/multiplexer 960 computes the final data bit LLRs $\{x_{data}\}$ as follows: $\{x_{data}\} = \{x_{data}^{N_{dd}} + x_{data1} + \tilde{x}_{data2}\}$, where $\{x_{data}^{N_{dd}}\}$ is the data bit LLRs provided by LLR computation unit 930 for the last detection/decoding iteration. A slicer 962 slices the final data bit LLRs $\{x_{data}\}$ and provides the decoded packet $\{\hat{d}\}$ for the packet being recovered. A CRC checker 968 checks the decoded packet and provides the packet status.

[0093] Referring back to FIG. 9A, the decoder LLRs $\{x_{dec}^{n+1}\}$ from FEC decoder 950 are interleaved by a channel interleaver 970, and the interleaved decoder LLRs are provided to detector 920. Detector 920 derives new detected symbols $\{\hat{s}_m^{n+1}\}$ based on the received symbols $\{r_m\}$ and the decoder LLRs $\{x_{dec}^{n+1}\}$. The decoder LLRs $\{x_{dec}^{n+1}\}$ are used to compute (a) the expected value of the interference (i.e., $E[\underline{\mathbf{s}}_i]$), which is used to derive $\underline{\mathbf{z}}$ in equation (12), and (b) the variance of the interference (i.e., $VAR[\underline{\mathbf{s}}_i]$), which is used to derive $\underline{\mathbf{Q}}$ in equation (11).

[0094] The detected symbols $\{\hat{s}_m^{n+1}\}$ for all received data symbol blocks from RX spatial processor 160a are again decoded by RX data processor 170b, as described above. The detection and decoding process is iterated N_{dd} times. During the iterative detection and

decoding process, the reliability of the detected symbols improves with each detection/decoding iteration.

[0095] As shown in equation (8), the MMSE detector response $\underline{\mathbf{w}}_i$ is dependent on $\underline{\mathbf{Q}}$, which in turn is dependent on the variance of the interference, $VAR[\underline{s}_i]$. Since $\underline{\mathbf{Q}}$ is different for each detection/decoding iteration, the MMSE detector response $\underline{\mathbf{w}}_i$ is also different for each iteration. To simplify receiver 150b, detector 920 may implement (1) an MMSE detector for N_{dd1} detection/decoding iterations and then (2) an MRC detector (or some other type of detector/equalizer having a response that does not change with iteration) for N_{dd2} subsequent detection/decoding iterations, where N_{dd1} and N_{dd2} can each be one or greater. For example, an MMSE detector may be used for the first detection/decoding iteration and an MRC detector may be used for the next five detection/decoding iterations. As another example, an MMSE detector may be used for the first two detection/decoding iterations and an MRC detector may be used for the next four detection/decoding iterations.

[0096] The MRC detector may be implemented with the term u_i, as shown in equation (6), where $\underline{\mathbf{w}}_{mrc,i}$ replaces $\underline{\mathbf{w}}_i$. As shown in equations (6), (9), and (12), the term u_i is dependent on the expected value of the interference, $E[\underline{s}_i]$. To further simplify receiver 150b, the term u_i may be omitted after switching from the MMSE detector to the MRC detector.

[0097] The iterative detection and decoding scheme provides various advantages. For example, the IDD scheme supports the use of a single rate for all data packets transmitted simultaneously via the N_T transmit antennas, can combat frequency selective fading, and may flexibly be used with various coding and modulation schemes, including the parallel concatenated convolutional code shown in FIG. 4B.

3. Rate Selection

[0098] For both single-carrier MIMO and MIMO-OFDM systems, the receiver and/or transmitter can estimate the MIMO channel and select a suitable rate for data transmission on the MIMO channel. The rate selection may be performed in various manners. Some exemplary rate selection schemes are described below.

[0099] In a first rate selection scheme, the rate for data transmission on the MIMO channel is selected based on a metric, which is derived using an equivalent system that models

the channel responses for the N_T transmit antennas. The equivalent system is defined to have an AWGN channel (i.e., with a flat frequency response) and a spectral efficiency that is equal to the average spectral efficiency of the N_T transmit antennas. The equivalent system has a total capacity equal to the total capacity of the N_T transmit antennas. The average spectral efficiency may be determined by (1) estimating the received SNR for each transmit antenna (e.g., based on received pilot and/or data symbols), (2) computing the spectral efficiency of each transmit antenna from the received SNR and based on a (constrained or unconstrained) spectral efficiency function, $f(x)$, and (3) computing the average spectral efficiency of the N_T transmit antennas based on the spectral efficiencies of the individual transmit antennas. The metric may be defined as the SNR needed by the equivalent system to support the average spectral efficiency. This SNR may be determined from the average spectral efficiency and based on an inverse function, $f^{-1}(x)$.

[00100] The system may be designed to support a set of rates. One of the supported rates may be for a null rate (i.e., a data rate of zero). Each of the remaining rates is associated with a particular non-zero data rate, a particular coding scheme or code rate, a particular modulation scheme, and a particular minimum SNR required to achieve the target level of performance (e.g., 1% PER) for an AWGN channel. For each supported rate with a non-zero data rate, the required SNR is obtained based on the specific system design (i.e., the particular code rate, interleaving scheme, modulation scheme, and so on, used by the system for that rate) and for an AWGN channel. The required SNR may be obtained by computer simulation, empirical measurements, and so on, as is known in the art. The set of supported rates and their required SNRs may be stored in a look-up table (e.g., LUT 184 in FIG. 8A).

[00101] The metric may be compared against the required SNR for each of the rates supported by the system. The highest rate with a required SNR that is less than or equal to the metric is selected for use for data transmission on the MIMO channel. The first rate selection scheme is described in detail in commonly assigned U.S. Patent Application Serial No. 10/176,567, entitled "Rate Control for Multi-Channel Communication Systems," filed June 20, 2002.

[00102] In a second rate selection scheme, the rate for data transmission on the MIMO channel is selected based on the received SNRs for the N_T transmit antennas. The received SNR for each transmit antenna is first determined, and an average received

SNR, $\gamma_{rx,avg}$, is then computed for the N_T transmit antennas. An operating SNR, γ_{op}, is next computed for the N_T transmit antennas based on the average received SNR, $\gamma_{rx,avg}$, and an SNR offset or back-off factor, γ_{os} (e.g., $\gamma_{op} = \gamma_{rx} + \gamma_{os}$, where the units are in dB). The SNR offset is used to account for estimation error, variability in the MIMO channel, and other factors. The operating SNR, γ_{op}, may be compared against the required SNR for each of the rates supported by the system. The highest rate with a required SNR that is less than or equal to the operating SNR (i.e., $\gamma_{req} \leq \gamma_{op}$) is selected for use for data transmission on the MIMO channel. The second rate selection scheme is described in detail in commonly assigned U.S. Patent Application Serial No. 10/394,529 entitled "Transmission Mode Selection for Data Transmission in a Multi-Channel Communication System," filed March 20, 2003.

[00103] The IR transmission techniques described herein may be implemented by various means. For example, these techniques may be implemented in hardware, software, or a combination thereof. For a hardware implementation, the processing units used at the transmitter for IR transmission may be implemented within one or more application specific integrated circuits (ASICs), digital signal processors (DSPs), digital signal processing devices (DSPDs), programmable logic devices (PLDs), field programmable gate arrays (FPGAs), processors, controllers, micro-controllers, microprocessors, other electronic units designed to perform the functions described herein, or a combination thereof. The processing units used at the receiver for receiving an IR transmission may also be implemented within one or more ASICs, DSPs, DSPDs, PLDs, FPGAs, processors, controllers, and so on.

[00104] For a software implementation, the IR transmission techniques may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. The software codes may be stored in a memory unit (e.g., memory units 142 and 182 in FIG. 1) and executed by a processor (e.g., controllers 140 and 180). The memory unit may be implemented within the processor or external to the processor, in which case it can be communicatively coupled to the processor via various means as is known in the art.

[00105] Headings are included herein for reference and to aid in locating certain sections. These headings are not intended to limit the scope of the concepts described therein

under, and these concepts may have applicability in other sections throughout the entire specification.

[00106] The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

WHAT IS CLAIMED IS: